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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,356	08/19/2003	Tsai-Sheng Gau	67,200-1053	8900

7590 09/07/2006

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EXAMINER	
DUDA, KATHLEEN	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 09/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/644,356	GAU ET AL.	
	Examiner	Art Unit	
	Kathleen Duda	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-19,25,26 and 29-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 10-19, 25, 26 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8, 10-19, 25, 26 and 29-31 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-8, 10-13, 15-19, 25, 26 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (US 6,064,466) in view of Beyer (US 4,33,794).

The invention is based on the relationship between subresolution and pattern density and resist thickness. A high pattern density minimizes the radiation that passes through a pattern mask. As the pattern density increases less actinic light is allowed through. The current system includes a multiple density portion pattern mask which is placed over the resist-coated substrate (col.1, 49-63). An exposure mask is adapted to account for surface irregularities of a wafer's surface in order to improve planarization. The value for the residual resist thickness depends on the light intensity, pattern density, development time and type of resist used. The initial resist

thickness is T (initial) (i.e. determining the first thickness). Semiconductor substrate 10 with (topography) feature 11, such as a line and space pattern, is coated with a layer of resist 12. A mask 15 with different light transmittance portion is aligned with the feature and a radiation source exposes the resist through the mask. The exposed resist is developed. The mask allows less than the full intensity radiation to fall upon some regions of the resist and therefore less resist is removed. After development the surface of the resist 22 over feature 11 and that over substrate 10 are equalized (thickness topography altered). Further the coating, exposing and developing steps may be repeated to further planarize the surface of the wafer. See col.2, 59-col.4, 2. and Figures 4A-E. The substrate may also have a narrow pit or indentation 31 (col.4, 3-25, Figures 5A-D). Mask of Figure 6A includes a simple opaque portion 34 and intermediate transmittance portions, such as subresolution pattern and portion 39 (col.4, 26-61). Semiconductor wafer 43 includes multiples trenches 41. This equates to a low pattern density over the non-trenched region and a high pattern density over the trenched region (i.e. first and second density). The mask portion above the thickest portion of the resist has the highest light transmittance. The level of the resist may be reduced to levels 44 (thickness portion covering and filling the vias) and/or 45 preparing the substrate for the next level of processing (col.4, 62-col.5, 33, Figures 7A-C).

Sato teaches that the above process may also be used to reduce the resist layer in the openings to a level below the substrate surface by adjusting the exposure time or mask transmittance. The reference does not disclose the method to further include an additional step of an etch process to produce a third thickness topography or an etchback to produce plugs filling the vias. Beyer teaches that it is conventional in the art to use an oxygen plasma etchback in order to fill and protect trenches with a resist plug (col.11, 6-15). It would have been obvious to one of ordinary skill in the art to use an etchback process to reduce the resist layer thickness and form via plugs in the method of Sato, instead of adjusting the exposure time or mask transmittance, because Beyer teaches that such an etchback process is conventional and known in the art and with the expectation that such a process while processing similar results would require an additional process step.

Sato teaches that the wafer includes multiple trenches openings with variable pattern density and does explicitly recite that these openings are vias as recited in claim 15. However trench openings and via openings are both conventionally found in the photolithography and semiconductor manufacturing art and their individual use would be dependent on the final device being manufactured. It would have been obvious to one of ordinary

skill in this art that the planarization method taught in Sato would be the same regardless of the name given to such openings.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato in view of Beyer as applied to claim 1 above, and further in view of Lewis (US 4,822,722).

Sato is silent on the method used to measure the initial resist thickness. Lewis teaches that the thickness of a photoresist layer is known to be measured using interferometry, profilometry and elipsometry (col.6, 34-44). It would have been obvious to one of ordinary skill in the art to use interferometry, profilometry or elipsometry to measure the initial resist thickness in the method of Sato in view of Beyer because Lewis teaches that these are all known suitable methods of resist thickness measurement.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato in view of Beyer as applied to claim 1 above, and further in view of Aronsatein (US 3,889,355).

Sato teaches exposing the photoresist by aligning a mask but is silent on the specific exposure method used. Aronsatein teaches that conventional resist exposure systems include contact printing, projection printing and step and repeat techniques (col.10, 3-10). It would have been obvious to one of ordinary skill in the art to expose the resist in the method of Sato in view of

Beyer using contact, projection or step and repeat techniques because Lewis teaches that these are all known conventional resist exposure systems.

Response to Arguments

6. Applicant argues that Sato does not provide a first and second density of features (claims 30 and 31 do not have this recitation). Sato depicts features before the photoresist is applied and these appear to be the same as the features depicted in figure 7A in the current application. Column 5, lines 1-14 of Sato discuss the different thickness of the resist and how it is compensated for in the exposure step.

Applicant argues that Sato does not teach determining the first thickness, just shows the different thicknesses between planar and non-planar surfaces. It is inherent that if one is to planarize a layer that the thickness of that layer must be determined before the planarization or too much material (or not enough) might be removed which would not lead to planarization. This thickness can be determined when the resist is first applied by spin speed.

Applicant argues that Sato does not teach an etchback process. Beyer was included in the rejection for its teaching of etchback.

Applicant argues that the references do not provide the solution to the problem which Applicant has solved. The prior art does not have to solve the same problem as the current application.

The Lewis and Aronsatein references were not discussed in Applicant's arguments.

Conclusion

7. Any inquiry concerning this communication should be directed to Examiner K. Duda at (571) 272-1383. Official FAX communications should be sent to (571) 273-8300.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff, can be reached at 571-272-1385.

Information regarding the status of an application may be obtained from the Patent Application Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kathleen Duda
Primary Examiner
Art Unit 1756